

Military

EMBEDDED SYSTEMS

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Duncan Young

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Embedded Operating Systems: Real Time, Linux, and Windows

June 17 • 2 pm EDT

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A recent photo exercise featured the aircraft carrier USS John C. Stennis (right), the USS Seawolf (front), and the Japanese destroyer JS Onami (left). USS John C. Stennis, weighing in at 97,000 tons, is propelled by two nuclear reactors and achieves speeds in excess of 30 knots. USS John C. Stennis typically serves as centerpiece within strikes comprising four to six additional ships – and transports a whopping 3 million gallons of fuel at a time for strike escorts and the carrier's own attached aircraft. Of course, this is a stark contrast to the still-formidable-on-foot 30 lbs of battery backups that ground soldiers often have to lug. However, a new, lightweight hybrid fuel system is providing a nonstop 72-hour fuel supply – while weighing in at only about 5 lbs. (See story, page 34.) [U.S. Navy photo by Petty Officer 3rd Class Walter M. Wayman]

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By Duncan Young

Rugged displays do more than meets the eye



Rugged display monitors are an essential part of every military system having a man in the loop. With applications ranging from command and control, combat systems, sensor/image displays, ground stations, shelters, training systems, all types of armored vehicles, and many more, these displays are the key decision-making interfaces between man and machine. Available in a multitude of resolutions and sizes, flat-panel Liquid Crystal Display (LCD) is the most popular choice due to its small space envelope, low power consumption, and enduring ability to be tailored to customers' specific environmental requirements. While primarily based on commercial LCD glass panels, a typical rugged display subsystem is often reengineered to meet a project's wide temperature range operation, readability, shock, vibration, and Electro-Magnetic Compatibility (EMC) requirements in addition to the potential integration of a touch screen or complete embedded computing subsystem.

Flat-panel display options

Flat-panel displays have completely displaced the bulky and power-hungry Cathode Ray Tube (CRT) in all but a few legacy military applications. LCD panels use a variety of associated technologies and offer excellent viewing characteristics as well as a wide operational temperature range when compared to LCDs available a few years ago. Color plasma displays commonly used in large screen, high-definition television have excellent picture quality and color spectrum but cannot meet the required temperature range, ruggedization levels, or low power dissipation of rugged LCD displays.

Flat-panel LCDs are an example of a commercial technology market segment still displaying healthy growth, receiving significant development investment, and continuing to evolve very rapidly in performance and affordability. Because the scope of application for rugged displays is diverse and the technology evolution fast, customers look for rugged displays that

meet their project-specific needs rather than selecting a particular technology up front. As a result, most rugged display subsystems incorporate some customization to precisely match them to the application. Variables include contrast ratio, video standard, size, shape, weight, mounting fixtures, power supply, temperature range, shock and/or vibration tolerance, or EMC. However, most of these individual specification items will be based on existing and proven technology offering fast turnaround and low risk to the user.

Unlike a household television that is operated and viewed in a very narrowly controlled environment, a rugged display might be required to operate in the open and must be readable in daylight or direct sunlight, requiring a much greater contrast ratio. In the case of LCDs, this is provided by cold cathode fluorescent backlighting with a wide dynamic range to provide the brightness required. For extended temperature range operation, the display must be heated at low temperatures to maintain its response times. Both the heating and lighting contribute to power dissipation, but improved efficiency and intelligent, selective control can be used to reduce a display subsystem's overall power dissipation to typically less than 30 W.

An LCD panel, being only a few millimeters thick, has little structural rigidity of its own. Additionally, the display cells might even distort under certain vibration conditions. To overcome this, the panel is bonded to a layer of toughened glass; this assembly can then be mechanically isolated within a chassis for additional protection. The layer of glass offers a base for the deposition of many types of coatings to improve the display's optical qualities. This glass will also incorporate an electrically

conductive layer for EMC control. Touch screens are also a popular addition to rugged displays, being more intuitive and easier to use with the military gloved hand than most typical keyboards.

Typical within a general purpose, PC-compatible range of rugged displays is the Sentinel from GE Fanuc Intelligent Platforms (Figure 1). Available in a range of sizes from 15" to 21", this type of rugged display subsystem is ideal for use in many naval applications, ground-based vehicles and shelters, and a variety of training environments.

Rugged LCD displays are excellent examples of how the military has profited from a strong commercial market. Just as LCD technology will continue its rapid evolution, so will the technologies required to ruggedize it.

To learn more, e-mail Duncan Young at young.duncan1@btinternet.com.

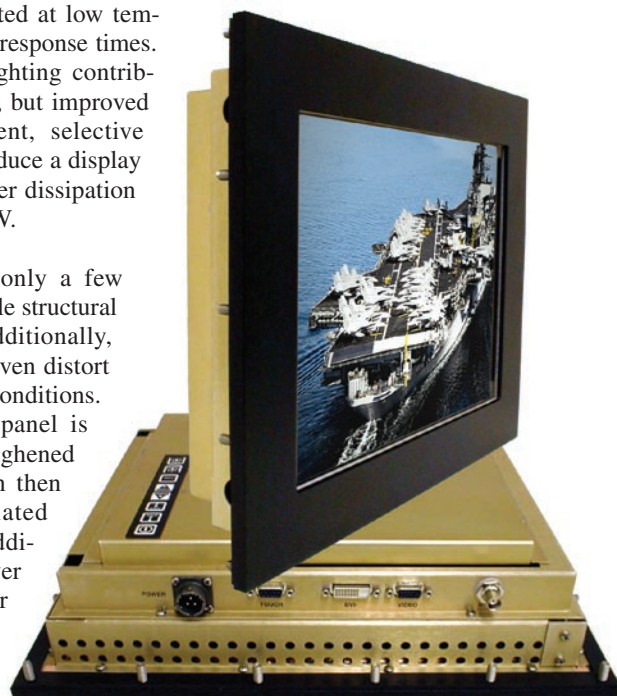


FIGURE 1: Typical within a general purpose, PC-compatible range of rugged displays is the Sentinel from GE Fanuc Intelligent Platforms.

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New mezzanine standard supports multi-GHz signal acquisition



By John Wemekamp



FPGAs continue to offer the ideal solution to the *front end* of embedded subsystem designs. They are used for a wide variety of applications ranging from the attachment of multiple analog I/O channels, often requiring continuous multi-GHz sampling rates, to pre- or post-processing of video or protocol stacks. However, this broad range of function and performance presents vendors of off-the-shelf FPGA products with the challenge of providing widespread flexibility with the fewest possible design variations. The FPGA Mezzanine Card (FMC) standard, ANSI/VITA 57, bridges the external world to an FPGA's I/O capability via advanced connector and signaling capabilities aligned with future I/O bandwidth expectations.

FPGAs and various applications

While FPGAs are now used for DSP in many very diverse applications, it is applications with many parallel and repetitive algorithms that really benefit. Surveillance, Signals Intelligence (SIGINT), and Electronic Counter Measures (ECM) are examples requiring the high channel count, I/O bandwidth, high performance, and low latency that FPGA-based technologies can provide. The latest generation of devices has the speed and complexity needed for continuous sampling of emissions within a baseband. To achieve this requires multi-Gbps bandwidth between the sampling A to D and FPGA. The L band, which lies between 1 and 2 GHz, is an example of such a band that might be of interest, requiring a minimum of 3G samples at 8-bit resolution, equating to 3 Gbps input bandwidth to cover the band completely. Low latency is also critical to these types of applications, either to switch to higher resolutions to refine a search or to react rapidly to certain external events, for example an ECM system's response to an emitter type.

FMC specifications

The FMC mezzanine has been developed to provide this high-bandwidth, close coupling between sensor and FPGA while also providing an added degree of I/O flexibility in a very small space envelope. Adopted by a number of COTS embedded computing vendors, FMC is a small form factor mezzanine that can be implemented in single or double widths, with the single width module measuring only 69 mm x 76.5 mm (2.72" x 3"). It uses a high-density I/O connector of 160 or, optionally, 400 pins between the FMC and its basecard. The connector supports single-ended or differential signaling at up to 2 Gbps plus a number of industry-standard 10 Gbps Multi-Gigabit Transceivers (MGTS). The smaller connector option supports one MGT pair while the 400-pin High Pin Count (HPC) option supports 10 pairs. The MGTS are intended for high-speed serial transmission links with protocol support provided by the FPGA. In this role, an FMC offers the ideal form factor for conversion between copper and fiber.

High-bandwidth paths from an FMC to its basecard make use of differential pairs. The transmission distance between an FMC

and its associated FPGA on the basecard is very short, making it practical to use both edges of a 1 GHz clock to transfer data, giving each differential pair a bandwidth of 2 Gbps. Clocking only 16 pairs at 1 GHz provides the 4 Gbps required by many baseband applications, still leaving many pairs free for additional functions or to provide similar high-speed data pipes to more than one FPGA. The FMC is compatible with many modular board-level standards such as VME, CompactPCI, AdvancedTCA, or VPX. Figure 1 shows an FMC module and one 3U and one 6U VPX board, each with one or two FMC module sites as offered by Curtiss-Wright Controls Embedded Computing (CWCEC). An FMC can be air- or conduction-cooled to suit a wide variety of environmental conditions. Similar to the XMC/PMC standard, FMC can have I/O signals routed via a front panel bezel or through the basecard and backplane for enhanced maintainability.

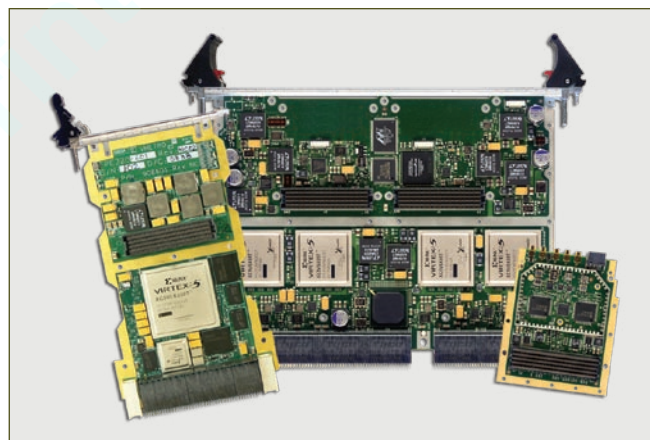



FIGURE 1: The FMC (pictured) is compatible with many modular board-level standards such as VME, CompactPCI, AdvancedTCA, or 3U and 6U VPX (also pictured).

The FMC and XMC/PMC, while apparently similar, are complementary in their application of FPGA technology to a DSP requirement. An XMC/PMC module will generally include both A to D and FPGA on a single mezzanine, using high-speed serial links such as PCI Express or Serial RapidIO to transfer results to the baseboard for additional processing or distribution. However, in some cases, FPGA-based applications are reaching beyond the capability of XMC/PMC to support increased I/O bandwidth, system latency, or power dissipation/cooling requirements. An FMC is better suited to applications such as SIGINT that require multiple FPGAs mounted on the baseboard with more than one multi-GHz path to distribute data, or other applications where more than one I/O function must be accommodated. An example is future multimode, multispectral sensors.

To learn more, e-mail John at john.wemekamp@curtisswright.com.



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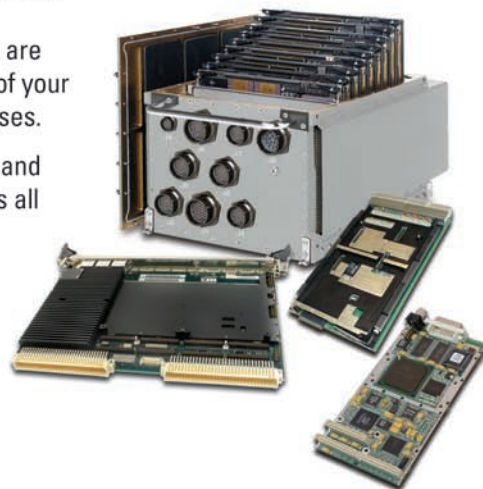
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Legacy algorithm harvesting for net-centric environments

The DoD has invested billions of dollars in mission-critical IT systems. These systems have been implemented for a number of years and feature an array of technologies. The following is a case study of the U.S. Army Guardrail Common Sensor (GRCS), a net-centric, SOA-based system providing critical intelligence information to the war fighter.

The heart of the U.S. Army Guardrail Common Sensor (GRCS) system is its emitter geolocation capability. This capability has proven to be one of the most reliable and accurate in the DoD Signals Intelligence (SIGINT) community. The

subject of our case study – GRCS – employs multiple emitter location algorithms and capabilities in an effort to optimize intelligence collection and emitter exploitation.

Accordingly, when migrating the GRCS algorithm, the first task was to understand the context in which the resulting SOA-based service would be deployed. The SOA system design paradigm makes software services available to network-centric applications. The role of SOA is to allow for information interoperability and exchange among producers and consumers. Relevant considerations for the migration included:

- Which type of integration will be used to make the new algorithm available in the target deployment environment?
- How will the migrated algorithm be integrated with the target environment's security and metadata models?

The deployment environment for the GRCS algorithm is the Distributed Common Ground System-Army (DCGS-A). Since GRCS contains multiple candidate emitter location algorithms, a critical step was determining which algorithm to harvest. The GRCS Hyper-Wide fix algorithm was a clear choice due to its low coupling with the rest of the GRCS system.

The next challenge was to harvest the Gauss-Newton emitter location algorithm. While more accurate than the GRCS Hyper-Wide fix algorithm, the Gauss-Newton algorithm is significantly more complex as a result of its distribution across several software modules. The first challenge we encountered was that the Gauss-Newton algorithm was not easily decoupled from the system. To add to the complexity, the algorithm has both C and Fortran components. This identified the algorithm as at least a Type 3 migration (partial application refactoring) effort. Because the Gauss-Newton algorithm was well documented, the opportunity for a Type 4 (full application refactoring) integration was possible. After discussing options with stakeholders, it was concluded that a clean port using modern tools for a Type 4 integration would be the preferred course of action.

Algorithm harvesting process

At the beginning of the GRCS algorithm harvesting effort, an industry survey was conducted to find relevant research on this topic. The most mature work was the Service-oriented Migration and Reuse Technique (SMART) supported by the Software Engineering Institute (SEI). SMART is a four-step process that describes the activities needed to analyze

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“ The GRCS migration effort used a modern spiral development approach to reverse-engineering legacy code, performing comprehensive reviews of algorithm documentation, and interviewing domain experts. ”

legacy systems and determine if they can be exposed as an SOA service. The first step is to work with stakeholders to capture project goals. Step two identifies candidate algorithms in the legacy system that meet stated goals. Step three evaluates migration costs against ROI of harvested algorithms. The fourth step is to prioritize the migration of each algorithm based on cost and stakeholder goals.

These four steps in the SMART process only represent a partial solution. The SOA service must still be designed, constructed, tested, and deployed. Our process on GRCS added a fifth step to support construction, test, and deployment needs. Step five is repeated for each algorithm and includes evaluation of migration options, test case and test data development, actual migration effort, and stakeholder progress reviews.

The GRCS migration effort used a modern spiral development approach to reverse-engineering legacy code, performing comprehensive reviews of algorithm documentation, and interviewing domain experts. Many opportunities to leverage modern computing technologies such as mathematic libraries for computationally intensive calculations and Web services/Java for platform-independent construction and deployment were used.

Lessons learned

The following lessons learned are valuable for any organization tasked with migrating legacy systems to a net-centric environment:

1. **Break the task in manageable spirals.** Breaking the effort into two- to three-month implementations provides a good opportunity for short-term goals to be achieved.

2. **Define specific goals for the reengineering/modernization effort.** By picking specific goals, designers can keep a narrow focus on the functionality required to migrate. This suits the unique opportunities of Web service migration well because by nature each service function should be automatic and decoupled (independent) from the rest of the system.
3. **Do not count reimplementing out.** When a piece of functionality is well documented, reimplementing can be very easy with the use of modern engineering tools.

4. **Build a good graphical UI/test harness.** The test harness with UI provides an easy mechanism to review work with project stakeholders and a concrete example of how to access the SOA service from consumer applications.

Tod Hagan is director of ISR Software Solutions at Modus Operandi, Inc. He served as the project lead for the design and development of critical software components on the U.S. Army Guardrail Common Sensor program. He can be reached at thagan@modusoperandi.com.

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Top 5 technologies for the warfighter

By Chris A. Ciufo, Editor

SFFs ... multicore ... secure RTOSs: You probably could guess these would make our Top 5 warfighter technologies list. But some of the others just might surprise you.

DoD photo by Master Sgt. Scott Reed, U.S. Air Force

Compiling our second annual list of Top Technologies for the Warfighter took more than six months and comprised nearly 50 interviews with various COTS suppliers and defense primes. Many of the purely civilian companies previously had no involvement with the defense industry. When we first spoke with some of these suppliers last Fall, just as the ugliness of the world's recession was beginning to hit, they couldn't possibly imagine gearing up to sell into "bombs, pointy-nosed things, or the war machine." Yet here we are in 2009, and several companies are now taking a closer look at Aerospace and Defense (A&D) applications as a possible revenue stream.

That's great news for the warfighter, as technologies such as partitioned cell phone microkernels promise big performance in power-constrained handhelds. Or there are new DSP-enabled EDA development suites ready to make high-density FPGA designs much easier while delivering faster silicon turns and lower system power. Some of this year's technologies were on last year's list because technology takes time to mature and get adopted in the civilian marketplace (Table 1). As well, we found that many of last year's categories began to merge, so we've narrowed the list to only 5 this year.

In no particular order, what follows is the 2009 list of technologies most likely to find their way onto a battlefield within the next three years, or those that will continue to keep being designed into A&D systems. (For some context to this list, check out the article entitled "Gates open to DoD budget reform" in the April 2009 edition of *VME and Critical Systems* magazine, or access www.vmecritical.com/articles/id/?3879).

1. RTOSs – Common Criteria, DO-178B, and ARINC-653

"It is actually possible to build high-assurance software," says Green Hills CTO Dave Kleidermacher, a recognized expert in all things RTOS. Kleidermacher and his team were highly instrumental in Green Hills' INTEGRITY-178 becoming the first software product to achieve EAL6+ (Evaluation Assurance Level) Common Criteria certification, earning the

2008's Top 10 Technologies

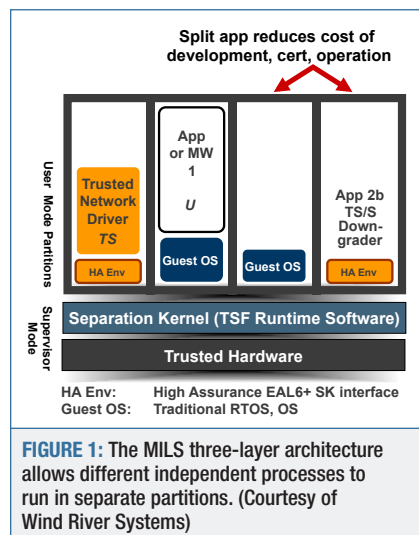
1	Solid-state disks
2	Multicore CPUs
3	CPU and system virtualization
4	Google – the great enabler
5	Software-Defined Radio (SDR)
6	FPGA devices and development tools
7	Simulation – cheaper training
8	Secure software – it's everywhere
9	Open standards
10	Open source software

TABLE 1: These were last year's Top 10 Technologies; some remain on this year's list. (See article at www.mil-embedded.com/articles/id/?2881.)

company an Editor's Choice award from this magazine (see www.mil-embedded.com/products/EditorsChoice). The NSA-sponsored, information technology oriented NIAP Common Criteria Evaluation and Validation Scheme is so rigorous that it took Green Hills and their sponsors more than 5 years to achieve this feat (using an RTOS design process that started over 10 years ago). Needless to say, it was a huge commitment. Only an EAL6+ High Robustness operating system is certified to protect classified information and other high-value resources at risk of attack from hostile and *well-funded attackers*. We're not talking about script kiddies or disgruntled teenagers; this phrase refers to state-sponsored and -organized cyber crime and terrorism.

With this certification in hand, Green Hills can legitimately boast that it has the most secure software of any kind in the universe (terrestrial and in space). And that's just what the company's competitors like Wind River Systems and LynuxWorks want to accomplish, too. Since Green Hills blazed the trail, the competition expects that their own MILS-oriented microkernels will have an easier time also achieving EAL6 certification once a program sponsors the effort. As of press time, NIAP's website lists Wind River's VxWorks MILS 2.0 in-process (aiming at EAL6) supported by CygnaCom Solutions, exactly as promised by the company's director of aerospace and defense marketing, Chip Downing.

Downing believes that better-architected security will be pervasive in RTOSs, although an RTOS need not be certified to EAL6+. The critical factor is a Multiple Independent Levels of Security (MILS) partitioned separation kernel that allows uncompromisable secure code to be run alongside inherently insecure code (such as Windows or Linux), as shown in Figure 1.



The secret to creating a MILS architecture is first implementing an ARINC-653 compliant kernel capability. Wind River's new VxWorks MILS 2.0, for instance, is based upon the company's VxWorks 653. This product boasts 120 design wins and is used on 35 different aircraft. While ARINC-653 is the bible on building partitioned OSs, there are other ways to skin a cat. Of note is DDC-I's Deos RTOS, originally created by Honeywell 14 years ago. Deos is a rate-monotonic RTOS that is completely configurable at run-time and doesn't rely on the rigid, time/space/schedule-wasting methodology of ARINC-653. And since Deos has been certified to DO-178B Level A on *dozens of commercial and military aircraft*, we believe that this now-COTS RTOS will become serious competition to Green Hills' and Wind River's flight- and safety-critical RTOS offerings.

Incidentally, ARINC-653 isn't the only game in town for high-reliability partitioned environments. We recently met with Open Kernel Labs (OK Labs), whose OKL4 embedded hypervisor brings virtualization to single-core ARM-based cellular handsets. Because of over-the-air data transactions and the growing consumer concern over security and identity theft, the OKL4 allows multiple OSs to run in secure partitions on a single CPU (Figure 2).

- Uniquely addresses virtual machines and individual applications or drivers
- Separating an application from the OS reduces its trusted computing base
- Native OKL4 applications are reusable with multiple OS
- Isolating applications does not require introduction of another OS
- Microkernel provides scheduling, isolation and communication services
- Communication between cells only allowed where explicitly authorized

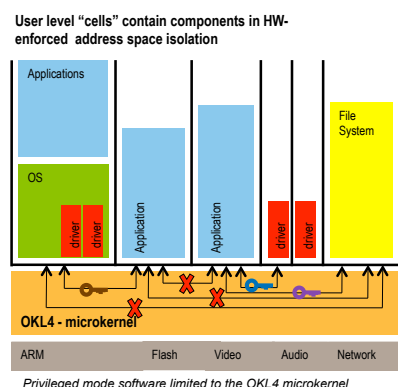


FIGURE 2: Who needs ARINC-653? Open Kernel Labs' OKL4 with Secure HyperCell technology is designed to allow secure virtualized partitions to run on ARM-based cell phones such as Motorola's Evoke QA4. (Courtesy OK Labs)

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2. and 3. Multicore CPUs; virtualization

Performance trumps power consumption, says Peter Cavill, general manager of the military and aerospace business unit at GE Fanuc Intelligent Platforms. He's talking about the "clever algorithm" needs of next-generation systems at handling the asymmetric threats of automatic target detection, authentication, alarming, tracking, and potentially autonomous weapons disposition. Crunching the math necessary to execute these algorithms requires lots of horsepower, possibly found in FPGAs, multicore processors, or even in General-Purpose computing on the GPU (GPGPU)¹. While Cavill doesn't see much beyond evolution in FPGAs, there's a notable shift away from Motorola/Freescale's Power Architecture in favor of Intel's x86.

Although Freescale was the first to design multicore CPUs such as Altivec PowerPCs into defense applications, Intel's dual-, quad-, and multi-core roadmap is compelling. Beyond Core i7 (Nehalem) CPUs and the latest Xeon 5500 series server

devices, Intel is also including MMU support, QuickPath interconnect to replace the FSB, and integrated graphics, which is handy for embedded training with no additional hardware footprint. The challenge, though, is cross-compiling Altivec code in legacy mil systems into Intel code, never mind the challenges with Endian-ness. Other specialty multicore CPUs that might find homes in defense include NVIDIA's Tesla multi-processor array.

And it's impossible to discuss multicore CPUs without discussing virtualization. Having started out in the enterprise space as a way to spread I/O resources across excess server CPU cycles, virtualization will soon become the *de facto* way to run multiple applications on desktop PCs. All those cores still need access to a fixed set of I/O peripherals, and virtual environments make it easy to share them. But in the military world, this allows multiple OS environments to also reside on the same CPU (still sharing cores and peripherals). Downing says that virtualization, coupled with the right partitioned RTOS,

allows combining legacy code with newer code, processors, and peripherals. In its simplest form, an older 1750 program could be plopped down on a new Intel SBC. Or a legacy Linux-based application running on a PowerPC could run in a virtual environment on a Core 2 Duo executing VxWorks. Virtualization and multicore CPUs abstract generations of software and hardware from each other: a perfect marriage in long life-cycle A&D systems.

4. and 5. Intel's Atom; Small Form Factors (SFFs)

Perhaps the biggest news items on this year's Top Technologies list are the Intel Atom processor and the proliferation of even more SFFs. Intel's Atom processor is targeted squarely at the low-power or battery-operated embedded market. Essentially a cut-down version of the company's Core Duo architecture with performance roughly equivalent to the previous generation laptop Pentium M (Dothan) family, the Atom family has all but created the new "Netbook" market segment (those sub-\$499 all-day laptops

¹ For more on the connection between GPGPUs and performance hikes, see "Maximizing GPGPU computing for embedded systems" by Alan Commike of Quantum3D (www.mil-embedded.com/articles/id/?3742).

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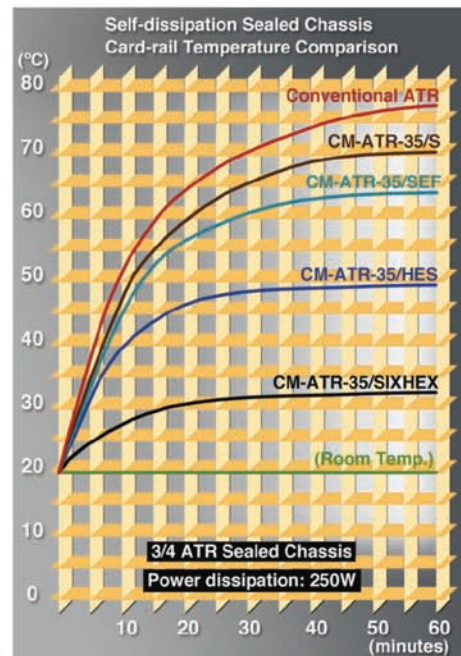
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powered by Windows XP or Linux and an Atom). According to IDC, Q42008 CPU shipments fell 11.4 percent from Q42007 to a still eye-popping \$6.78 billion. Intel had about 82 percent market share (while AMD was nearly 18 percent and VIA had a mere 0.4 percent), but the Atom is credited with saving nearly 20 percentage points. IDC estimates that without it, worldwide CPU shipments would have declined by 21.6 percent year over year. That makes the Atom, launched in Q2 2008, a huge success.

What makes Atom so compelling for defense applications is that it's a PC-

compatible CPU designed for low-power, long life-cycle, extended temperature embedded systems. Many of the Atom Z5xx flavors are on Intel's seven-year roadmap, and all of them are under 2.5 W. The Z500 (512K cache, 800 MHz, 400 MHz FSB) sips a mere 0.65 W but isn't on the long life-cycle roadmap. Still ... the Size, Weight, and Power (SWaP) potential is amazing. Intel's stated goal with the Atom is targeting "MIDS" – the estimated tens of millions of mobile Internet devices. In the Notebook space, Intel even created a Linux ecosystem called Moblin (<http://moblin.org>). Countless embedded apps from this organization

cry out for military deployment. And why not? Both hardware and software are designed for all-day connectivity running on batteries. Sounds like a soldier's or a Marines' dream: to stop slinging extra batteries instead of extra ammo.

In the SFF hardware arena, PC/104 and its progeny once ruled the roost. But while getting even a Pentium M on this form factor was a challenge due to cooling, the Atom enables so many new SFF sizes that we can't list them all here. Sizes like Mini- and Nano-ITX, Pico-ITXe, COM, SUMIT, and now COMIT. This latter SFF, recently announced by the SFF-SIG (sff-sig.org), is a credit card-sized Computer-On-Module (COM) designed with high-speed COM Interconnect Technology (COMIT) for USB3 and PCIe 2.0. Figure 3 shows what's being dubbed the 62 x 75 mm *SFF-COM*, pictured here with an Intel Atom.



FIGURE 3: A picture of the SFF-COM card showing its size relative to a credit card: This is the bottom side of the board and shows the COMIT 240-pin connector at the top. (Courtesy WinSystems)

Wrapping it all up

No one knows the future, considering all the economic conundrum and proposed defense spending shifts. So there's no telling which Top 5 technologies the coming 12 months will bring. But what we do know for now is that the warfighter's technology needs are or soon will be met with flying colors by this year's Top 5 trends: RTOSs that are soaring to DO-178B, Common Criteria, and ARINC-653 levels; amped-for-higher-horsepower multicore CPUs and their logical counterpart: virtualization. And, of course, last but definitely not least: The Intel Atom and myriad SFFs will be instrumental in aiding warfighters on land, sea, or air well into the foreseeable future; we wouldn't be surprised if one of their myriad incarnations even appears on next year's list. ➤

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Exploiting advanced imagery with a standards-based network architecture

By Thomas Roberts

Modern military forces rely heavily on sensor-based imaging systems, but extracting only the most valuable imagery information and getting it into the right hands quickly can be challenging. However, a new Converged Sensor Network (CSN) Architecture is delivering critical sensor-based information to users on the tactical edge.

New generations of sensor-based imaging systems are generating invaluable information for our military forces, using increasing numbers of both manned and unmanned platforms. Video imagery is now highly detailed, but it's not just video; Synthetic Aperture Radar (SAR) and Electro-Optic Infrared (EO/IR) sensors can create detailed images at night and through cloud cover. Soon Hyperspectral Imaging (HSI) and Laser Radar (LADAR) will additionally advance our imaging capabilities. These technologies operating from new platforms provide an unrivaled ability to gather detailed imagery of any geography, giving our armed forces both strategic and tactical advantages in current and future conflicts.

That is all good, but a significant challenge remains: How do we extract truly valuable information from all that imagery and then get that information to the people who really need it, when they need it? Imagery by itself is often of little value; for example, seeing tire tracks in the soil outside a village is not too important, but knowing they were not there the previous evening may be critical information. And the person who needs that information is probably not an analyst in the Pentagon, but a war fighter preparing to enter the village.

A flexible network or a network of networks is needed to link sensor systems to the ultimate users of the information, and the Converged Sensor Network (CSN) Architecture is delivering this capability.

Data imaging challenges

This challenge of extracting and delivering useful information actually has several dimensions. First, there is the issue of bandwidth limitations in the data links that provide the transmission backbone from a sensor platform to a ground station. Currently deployed data links cannot transmit the full data streams generated by advanced sensors. Improvements in data communications will increase available bandwidth, but data links will still be overwhelmed by ever-larger streams of raw data from new generations of sensors.

A second issue is the difficulty of communications between different types of platforms and systems. Too often, information has to flow all the way up, then down different chains of command because there is no good way to move imagery directly from point A to point B, even though both are out on the tactical edge.

And lastly, there is the issue of merging and synthesizing information from multiple sensors. For example, combining infrared

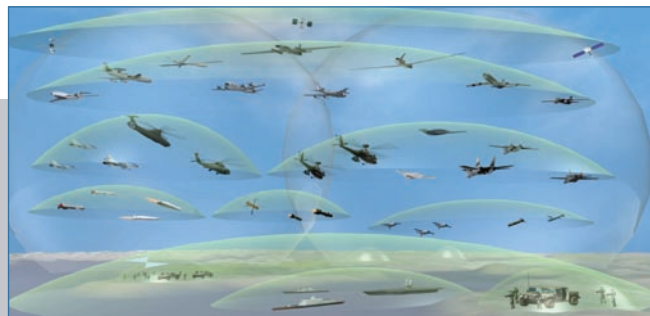


FIGURE 1: The CSN Architecture vision encompasses a flexible network of networks.

and radar images may give real insight into what is happening at a particular place, but allowing that combination to happen quickly is very difficult with today's systems. Because the infrared and radar images are produced by separate systems, focused human intervention is needed to create combined coverage of a specific physical location.

Addressing these interrelated issues requires a new paradigm for processing and communicating sensor-generated data. Military operations need flexible networks of intelligent nodes that can process imagery, share that information, and deliver it quickly wherever it is needed (Figure 1).

Converged Sensor Network Architecture

The CSN Architecture provides a flexible, standards-based approach to creating such a network, using a novel approach for digital signal processing that conjoins the agility of cluster computing with sensors at the tactical edge. Rather than funneling all network traffic through a host processor, the CSN Architecture makes each sensor and its associated embedded computing assets look like a standard cluster on an IP-based network.

To enable the CSN Architecture, Mercury Computer Systems has introduced a set of SigmaNET software and hardware components, including:

- Interconnect software that upgrades the RapidIO fabric to support high-performance Ethernet tunneling.
- A gateway hardware module that bridges a RapidIO subsystem with interconnect software installed on an external 10 GbE network. The gateway module is responsible for forwarding Ethernet traffic into and out of a RapidIO subsystem.
- Failover software that enables a redundant RapidIO fabric to isolate faults and recover from failures, including failures in an external network, via routing changes. +

Thomas Roberts is a product marketing manager at Mercury Computer Systems. He has more than 25 years of experience in systems engineering and technical marketing with IBM, Nixdorf, Data General, Digital Equipment, and Compaq. He holds a BS in Engineering from Cornell University and an MBA from the University of Kansas.

Enabling AdvancedTCA to support truly distributed processing applications

By Chris Eckert

An important limitation has previously prevented AdvancedTCA from establishing itself even more widely as the communications architecture of choice for next-generation networks. That limitation is PCI Express control architecture definitions. However, this challenge can be overcome through an understanding of serial link technologies including the impact of PCI Express bridging and reference clock shortcomings, along with corresponding open systems standards and a universal AMC.

The Advanced Mezzanine Card (AdvancedMC or AMC) specifications published by PICMG define a small form factor module that is easily integrated into either a host carrier board or into a dedicated chassis (Figure 1 – see also www.picmg.org/pdf/AMC.0_R2.0_Short_Form.pdf). The AMC form factor was originally defined for deployment in NEBS-compliant telecom systems on either an AdvancedTCA carrier board or in a MicroTCA platform. AdvancedMC modules are sized to contain all of the hardware and firmware required for a system element, such as a processor node, I/O port controllers, or storage devices.

Simple engineering rules define aggregation of AdvancedMCs into larger physical and functional system architectures. However, when deploying AdvancedMCs in some applications, including communication gateways, PCI Express control architecture definitions present challenges. An examination of serial link technologies – including the impact of PCI Express bridging and reference clock limitations plus corresponding open systems standards – is presented. Meanwhile, a Universal AMC is key.

The roles of serial link technologies

The AMC specification suite includes definitions for high-speed serial interconnect among modules using multiple serial link technologies, including Ethernet, PCI Express, and Serial RapidIO. Industry practice tends to assign application or user plane data traffic to the Ethernet or Serial RapidIO infrastructure and local control plane traffic to the PCI Express infrastructure.

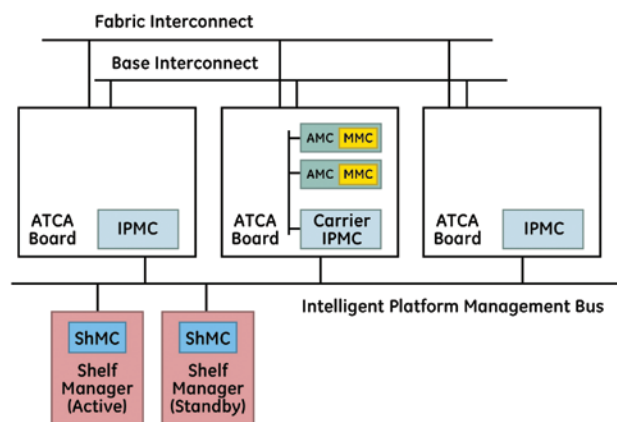


FIGURE 1: Simplified AdvancedTCA architecture: Each AdvancedTCA board can be given a unique “personality” dependent upon the AdvancedMC module mounted on it.

Ethernet and Serial RapidIO network definitions are based on a loosely coupled architecture model, where each node in the network has the resources required for its assigned function, and data traffic on the network is confined to application data packet transfers.

The PCI Express control architecture definitions are carried forward from the PCI local bus specifications originally published in the 1990s. This has permitted evolution of hardware

platforms for application software designed to utilize PCI resources for data transfers. Under these definitions, one node is defined as the *Root Complex* and contains a host processor plus software to manage all other nodes (called *End Nodes*) on the shared bus. The host processor is assumed to have complete control over all of the resources at each target node, and the bridging interface between the host processor and an End Node is called a *Transparent Bridge* (TB), as depicted in Figure 2.

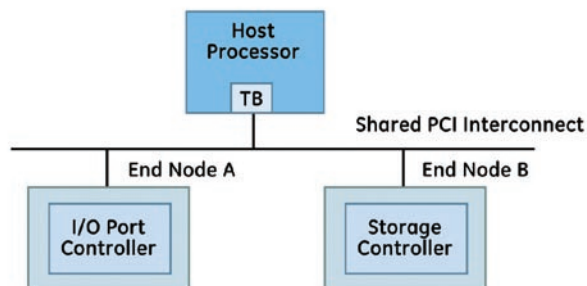


FIGURE 2: When transparent bridges are powered on, they learn the topology of the network by analyzing the source address of inbound frames from all attached nodes.

In contrast to Ethernet and Serial RapidIO, PCI Express interconnect is based on a tightly coupled network model where the host processor at the Root Complex is enabled to directly access and utilize all resources at intervening switches and at each End Node. The host processor is the master of the physical interconnect and controls all data transfer operations; the other nodes in the network are functional slaves and respond to commands issued by the Root Complex. Further, the host processor expects to have direct control over all hardware resources in the End Nodes.

While this architecture is very efficient in traditional PCI environments such as ATX motherboards, it does create significant restrictions for application platforms that require embedded processing nodes with local memory or I/O resources at End Nodes in a distributed processor architecture. An understanding of PCI Express's limitations and composition is necessary to remedy the dilemma.

PCI Express interconnect architecture limitations

PCI Express serial link specifications published by the PCI Special Interest Group (PCI-SIG) provide detailed descriptions of the voltages, line coding, embedded reference clock definitions, and other electrical attributes of these serial links. All PCI Express serial link configurations are defined as bidirectional connections using one or more pairs of unidirectional serial links. PCI Express interfaces at plug-in modules may optionally include a 100 MHz reference clock, which is used for enhanced link synchronization purposes and in spread spectrum environments.

Importantly, the original PCI (and PCI Express) specification did not foresee any requirement for multiple processors to exist within the same PCI domain, so provision for this capability was not made. In order to support these distributed processing architectures, each application processor node includes local memory and peripheral resources that the application processor needs to operate autonomously without interference from the host processor.

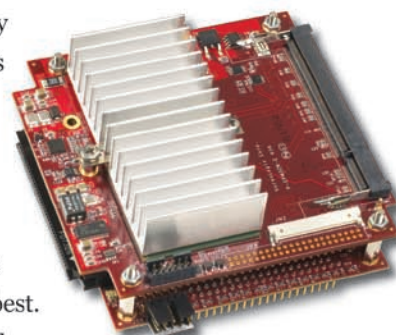
The Non-Transparent Bridge (NTB) was introduced by silicon vendors to address these platform architectures. At an NTB, the

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host processor is assigned a small shared memory window at the applications processor, which contains both hardware registers and a small amount of physical memory. The host processor and applications processor interact with each other using data block transfers through this memory window, following a specified exchange protocol defined in the PCI specifications. More importantly, the host processor has no knowledge of, or access to, any other resources at the applications processor. Typical architectural design practice is to provide an NTB at the embedded application processor node rather than at the host processor node (Figure 3).

Support for embedded applications processors at End Nodes was addressed in PICMG for CompactPCI systems with the introduction of specifications supporting nontransparent bridging on the backplane CompactPCI bus. However, that effort was not extended to encompass the PCI Express infrastructure in the AdvancedTCA/AMC domain.

AMC.1 module definitions: To the rescue?

The PICMG AMC.1 specification provides signal assignments for the optional 100 MHz PCI Express reference clock. In typical platform applications, each PCI Express AdvancedMC module receives the reference clock from a central clock synchronization circuit. However, the AMC.1 specification does permit the primary Root Complex AMC module to source the reference clock as the master of the PCI Express interconnect. Management configuration options for the reference clock are limited to interface enable/disable.

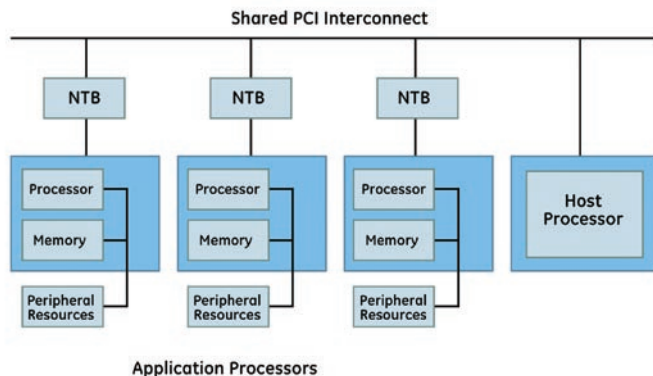


FIGURE 3: NTBs are provided at the applications processor node to shield local processor resources from the host processor.

The PICMG AMC.1 specification also defines assignment of PCI Express serial links on the AdvancedMC module as well as some host system interconnect requirements. The AMC.1 specification allows the assignment of one x8 PCI Express serial link to AMC “fat-pipe” carrier ports 4 to 11 and includes definitions for managing this interface by the platform’s Shelf Manager through the module’s Module Management Controller (MMC) on the AdvancedMC module. In standard AdvancedMC host systems, this PCI Express link is connected to one port on a central switch located on, for example, the MicroTCA Carrier Hub (MCH) in a MicroTCA platform. Management configuration options for the serial link are limited to interface enable/disable operations and

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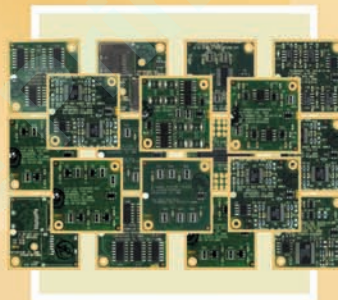
1

**Select an
FPGA-based
Carrier**



2

**Choose I/O
Conversion
Modules**



3

**Assemble
with IP Core
and ECM Code**



Patent Pending

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lane configuration. All configuration operations are implemented by the MMC prior to enabling power for the application circuitry on the AdvancedMC based on configuration data received from the platform's Shelf Manager.

Transparent bridging is assumed for the Root Complex and all End Node AdvancedMCs, as well as at all switch port interfaces. The AMC.1 specification does provide an option for nontransparent bridging at the central switch for an interface port that hosts the secondary Root Complex. However, there is no functional specification or MMC configuration mechanism defined for providing nontransparent bridging at an End Node containing an embedded processor circuit.

Bridging the gap

Work done by GE Fanuc addresses both the bridging and reference clock configuration shortcomings of standard AdvancedMC modules, defining a serial link bridging function and a reference clock interface that is configurable by the MMC during power-up initialization of the AdvancedMC module. The AMC.1 Universal AMC PCI Express interface architecture defines a serial link bridging function and a reference clock interface configurable by the MMC during power-up initialization.

A universal bridge is included with the PCI Express port controller, and this may be implemented at the processor core or on a System-on-Chip (SoC) device that includes the processor itself, a memory controller, processor peripheral resources, and other

I/O port controllers. Alternatively, the bridge function may be provided on a discrete device, such as a port switch.

In either configuration, the bridge is configured in transparent or nontransparent mode using inputs controlled by the MMC before power is applied to the processor core during hardware initialization. As defined in the AMC.1 specification, Root Complex AdvancedMC modules are always defined to have a transparent bridge, with nontransparent bridging for the secondary Root Complex module managed at the central switch. Storage or I/O End Node AMC modules controlled by the Root Complex typically do not include a bridge. End Node AdvancedMC modules with an embedded processor do have an NTB.

A bidirectional PCI Express reference clock interface is included in the GE Fanuc interface definition. This interface is configured to be either an input from the carrier or an output to the carrier, depending on the overall reference clock architecture in the host system. The secondary Root Complex AdvancedMC module and all End Node AMC modules are configured to receive the reference clock. The primary Root Complex AdvancedMC module may be configured to either source the reference clock or receive it from a separate clock synchronization circuit.

These definitions are implemented on the GE Fanuc ASLP11 Processor AMC, and are provided to the MMC by a Shelf Manager during the initialization sequence using standard

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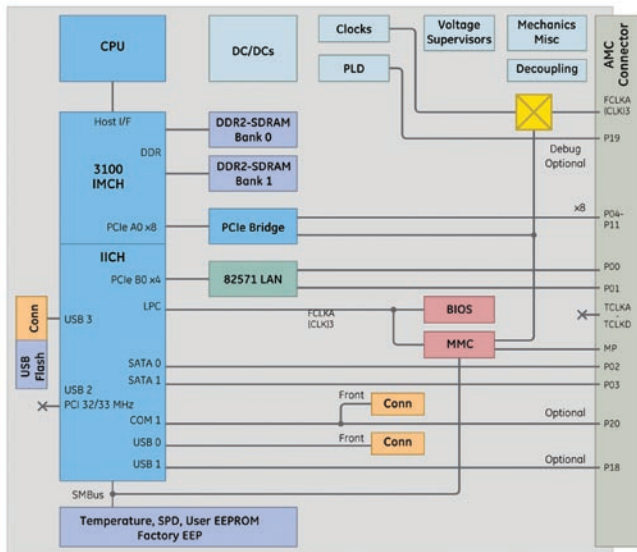


FIGURE 4: The AMC.1 Universal AMC PCI Express interface architecture defines a serial link bridging function and a reference clock interface configurable by the MMC during power-up initialization.

module management operations (Figure 4). The MMC deployed on the ASLP11 includes firmware to receive configuration data pertaining to these functions from the platform Shelf Management Controller (ShMC) and set appropriate hardware resources during the module's hardware initialization.

It can be done

AMC host system architectures based on PCI Express switch fabrics use the PCI Express infrastructure to transfer control data, application data, or both types of data between tightly coupled nodes in the host system. However, the PICMG AMC.1 specification does not address the bridging and clock issues that need to be resolved if the requirement is to deploy a truly distributed processing platform. The AMC.1 Universal AMC module alleviates these issues with its universal bridging and reference clock management infrastructure.



Chris Eckert is responsible for advanced product definition of processor boards and SBCs for GE Fanuc Intelligent Platforms, where he is senior system architect and principal engineer. Chris, a registered Professional Engineer, has developed board- and system-level products for a wide range of military, avionics, communications, and industrial control applications during the past 25 years. He holds a BS in Computer Engineering from Iowa State University and an MSEE from Duke University. He can be contacted at chris.eckert@gefanuc.com.

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We Put the State of the Art to Work

Ruggedized MicroTCA gears up for deployment

By Bob Sullivan and James Doyle

Amidst today's clamor for small, rugged form factors with built-in-test, network-centric performance, and lower cost, MicroTCA is proving itself a viable choice. Meanwhile, PICMG continues to develop ruggedized MicroTCA standards aimed to help developers navigate the temperature, shock, vibration, and cooling issues sometimes encountered with designing in MicroTCA.

Over the past two years, many things have changed: The United States has a new administration in the White House, a global economic crisis is underway, and the needs and desires of the embedded computing marketplace have evolved accordingly. And all of these factors are interrelated when it comes to the growing government and military interest in smaller form factors like MicroTCA.

Lower costs and more scalable designs have lofted MicroTCA to a position of interest among some of the world's leading technology transfer laboratories. Their interest includes both benign and rugged applications. In fact, some early adopters are already using ruggedized MicroTCA systems for proof of concept development and early field trials in net-centric communications and C4ISR rugged applications. Given the fact that the three largest military programs associated with the Navy, Marines, and Air Force these days are network-centric open system platforms, it is no wonder that many in the industry are focused on this technology.

Additionally, MicroTCA successfully resolves technical/program challenges and needs such as built-in-test, network-centric performance, and lower cost. Meanwhile, PICMG continues to develop its ruggedized MicroTCA standards to help developers navigate through the temperature, shock, vibration, and cooling issues sometimes encountered with designing in MicroTCA.

MicroTCA resolves technical challenges

Many programs require extensive built-in-test. Because existing rugged system architectures such as VPX, VXS, and VME do not currently support an open multivendor built-in-test capability, customers are locked into a single vendor's proprietary solution, or they need to customize the COTS products. MicroTCA's robust system management architecture inherently supports open multivendor built-in-test capabilities out-of-the-box, which is a significant customer benefit.

Additionally, many rugged network-centric applications are based on com-

mmercial networking technology such as Ethernet and WiMAX, but existing rugged system architectures such as VPX, VXS, and VME are not commonly used for commercial network-centric applications. AdvancedTCA is in widespread use in commercial network-centric applications and has already been adopted for many benign-environment communications-centric military applications. MicroTCA is derived from AdvancedTCA, so it enables easy porting of these applications from AdvancedTCA to MicroTCA for small form factor applications.

Meanwhile, many rugged network-centric applications require small form factors for applications that are tightly constrained by size, weight, and power. MicroTCA is very attractive for these applications because of its small size, light weight, and low power.

Our current economic conditions will require many applications to reduce cost while providing new capabilities. MicroTCA's commercially based roots mean lower cost, particularly in network-centric rugged applications.

DoD photo by Staff Sgt. Vanessa Valentine, U.S. Air Force

MicroTCA.1 performance criteria	MicroTCA.1 performance classes	Levels	Module retention
Operating temperature	XT1	-40 °C to +70 °C	
	XT1L	-40 °C to +55 °C	
Operating vibration	XR1	IEC 61587-1 "Vibration Test Conditions, performance level DL3" Sinusoidal vibration at 3 g rms	
	XR2	ANSI/VITA 47 class V2 vibration test requirements Random vibration, 5 Hz to 100 Hz PSD increasing at 3 dB/octave, 100 Hz to 1,000 Hz PSD = 0.04 g ² /Hz, 1,000 Hz to 2,000 Hz PSD decreasing at 6 dB/octave ~8 g rms	Requires additional retention device with new screw-in type faceplates
Operating shock	XR1	IEC 61587-1 "Shock Test Conditions, performance level DL3" 25 g, 15 msec shock Note that this exceeds the shock levels in ANSI/VITA 47 class OS1.	

TABLE 1: The MicroTCA.1 specification addresses a first level of ruggedization for air-cooled applications based on existing MicroTCA.0 and AMC form factors.

MicroTCA gets ruggedized PICMG-style

PICMG is developing a series of MicroTCA specifications addressing several levels of ruggedization: PICMG MicroTCA.1 covers rugged air-cooled MicroTCA, PICMG MicroTCA.2 expands this to hardened air-cooled MicroTCA, and PICMG MicroTCA.3 addresses conduction-cooled MicroTCA.

PICMG MicroTCA.1:

Rugged air-cooled MicroTCA

The PICMG MicroTCA.1 draft specification is in the final stages of approval; this specification addresses a first level of ruggedization for air-cooled applications based on existing MicroTCA.0 and Advanced Mezzanine Card (AdvancedMC or AMC). MicroTCA.1 also includes provisions for rear I/O connections. Table 1 shows ruggedization levels for MicroTCA.1.

Release of the PICMG MicroTCA.1 specification is expected early in the second quarter of 2009, as this article goes to press. This specification will enable AMC and MicroTCA suppliers to provide interoperable ruggedized products and technologies for extended temperature and mobile applications in industrial, outside plant telecom, and aerospace environments. Although not specifically targeting military applications, MicroTCA.1 products meeting XT1 and XR2 ruggedization levels are suitable for military applications where many rugged air-cooled VME64x and CompactPCI products are used today.

PICMG MicroTCA.2:

Hardened air-cooled MicroTCA

Work will begin in earnest on the PICMG MicroTCA.2 specification once the MicroTCA.1 specification is released. MicroTCA.2 is aimed at providing more rugged two-level maintenance modules

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PICMG MicroTCA.3:

Conduction-cooled MicroTCA

Work is well underway on the PICMG MicroTCA.3 specification's development. Environmental specifications target the conduction-cooled levels found in ANSI/VITA 46 (VPX). A few of the key criteria are included in Table 2.

MicroTCA.3 adds conduction-cooled "clamshells" around existing MicroTCA

ANSI/VITA 47 performance classes	ECC2	ECC3	ECC4
Operating temperature (card edge)	-40 °C to +55 °C	-40 °C to +70 °C	-40 °C to +85 °C
Operating vibration: V3	Random vibration, 5 Hz to 100 Hz PSD increasing at 3 dB/octave, 100 Hz to 1,000 Hz PSD = 0.1 g ² /Hz, 1,000 Hz to 2,000 Hz PSD decreasing at 6 dB/octave ~12 g rms		
Operating shock: OS2	40 g, 11 msec shock		

TABLE 2: MicroTCA.3's environmental specifications target the conduction-cooled levels found in ANSI/VITA 46 (VPX).

and AMC printed circuit modules. To provide space for the thermally conductive clamshells and wedgelocks, the conduction-cooled modules grow about

20 mm as compared to the single- and double-width AMC and MicroTCA.0 module sizes.

The MicroTCA.3 3D mechanical models, tolerance analyses, and drawings are already completed, so the most significant work remaining is the planned extensive environmental testing of the conduction-cooled modules and connectors.

The proof is in the test

Testing on MicroTCA.1 and MicroTCA.3 has already begun, and results are publicly available on PICMG's website at www.picmg.org. More testing is also in the works.

Ruggedized MicroTCA test data indications

Air-cooled MicroTCA.1 shock and vibration testing has been performed by Harting and Schroff. This testing shows that:

- Air-cooled MicroTCA modules with edge fingers and MicroTCA backplane connectors can withstand the XR1 and XR2 shock and vibration levels.

Conduction-cooled MicroTCA.3 shock and vibration testing has been performed by Harting. This testing indicates:

- Conduction-cooled MicroTCA modules with edge fingers and MicroTCA backplane connectors can withstand the higher ANSI/VITA 47 conduction-cooled shock and vibration levels.
- MicroTCA connectors operate reliably with the system-level, conduction-cooled mechanical tolerances and offsets of wedgelock clamping.

Planned testing for MicroTCA in rugged apps

There is some concern regarding the AMC edge finger connector reliability in rugged air-cooled or conduction-cooled

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“ There is some concern regarding the AMC edge finger connector reliability in rugged air-cooled or conduction-cooled applications. Testing performed to date has been very encouraging, but a thorough environmental test report is needed to overcome these concerns. ”

applications. Testing performed to date has been very encouraging, but a thorough environmental test report is needed to overcome these concerns.

PICMG has contracted with Contech to finalize the test procedure for conduction-cooled MicroTCA module and connector testing. An extensive suite of environmental tests, patterned after the work that Contech performed for VITA 46 modules and connectors, will be conducted. (VITA 46 test report results are available at www.vita.com.)

This planned environmental testing will provide a solid baseline for using MicroTCA in rugged applications.

Advantages of MicroTCA

AdvancedTCA has already been adopted in many benign-environment communications-centric military applications. MicroTCA is derived from AdvancedTCA, so it allows scaling of applications from AdvancedTCA to MicroTCA for small form factor applications. MicroTCA is very attractive for these applications because of its built-in-test, net-centric performance, low cost, and ability to overcome temperature, shock, vibration, and cooling challenges.

In our current economic climate, many applications will be expected to decrease in cost yet provide new capabilities. MicroTCA, with its commercially based roots, is well positioned for design wins in network-centric rugged applications.

It has taken a while for the industry to get to this point. Now that the PICMG Rugged MicroTCA.1 specification is soon slated for release, suppliers can move ahead with rugged and extended temperature roadmaps. The promise of rugged MicroTCA will only be realized if MicroTCA product suppliers move quickly to offer rugged and extended temperature versions of their products. Emerson and Hybricon are committed to this effort. ⊕



Bob Sullivan is vice president of technology at Hybricon, where he is responsible for keeping abreast of industry

technology trends, setting technical direction for the company, and defining technical approaches to solve challenging problems for key customers. He is active on both the VITA/VSO and PICMG technical standards committees. Recently, he served as cochair and draft editor for the MicroTCA Ruggedization SIG, and he is currently secretary of the MicroTCA.3 committee. He can be contacted at bsullivan@hybricon.com.

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Unique COTS applications of the double-conversion on-line UPS

By Michael A. Stout

Engineers often only implement the use of double-conversion, on-line UPS technology when they have a battery backup requirement. The technology frequently offers many more capabilities that are not often realized or understood. The capabilities may vary from UPS manufacturer to manufacturer and may not be readily clear in the manufacturer's datasheets or sales materials. When understood, the true capabilities of the on-line UPS may be a real problem-solver for the systems design engineer.

As our military and government continue facing the difficulties of protecting citizens and soldiers, an emphasis is placed on rapid implementation of newly developed technology. One example is the military's push for immediate technology-based systems for the Improvised Explosive Device (IED) problem in Iraq and Afghanistan. More recently, Homeland Security has contracted with companies to develop advanced equipment to protect U.S. borders. These systems, along with a multitude of others, must be deployed domestically and throughout the world. To speed their development and deployment, engineers have incorporated into these systems COTS computers, power supplies, and other electronics that are designed to operate from 120 VAC domestic power. At first, their choices of power-compatible equipment may seem limited as the domestically available COTS equipment may have to operate from international voltages and frequencies. Due to the sophisticated design of this equipment, ultra-clean, reliable power is demanded.

Embedding existing COTS double-conversion on-line Uninterruptible Power Supply (UPS) technologies can assist equipment manufacturers and engineers with a low-cost solution to these power problems. This type of UPS technology is very flexible as it can provide no-break power backup, in addition to offering superior AC output voltage regulation; surge, transient, and overvoltage protection; frequency regulation; frequency conversion; input power factor correction; and with some models, phase conversion.

Overview of double-conversion on-line UPS design

The double-conversion on-line UPS is designed with a continuous-duty inverter circuit. The inverter produces new sinewave output power while operating from the incoming utility source, or when not available, from its internal or external battery sources.

The incoming Alternating Current (AC) utility or generator power is rectified to an unregulated Direct Current (DC) and filtered. The batteries are also connected at this point. The unregulated DC from the utility or the DC from the batteries is fed to a regulating boost chopper or DC-DC converter circuit. This provides regulated power at a suitable voltage to the input of the DC-AC inverter circuit. The DC-AC inverter circuit then regenerates clean, tightly regulated, true sine-wave AC power for use by the connected equipment. An additional bypass circuit is provided, allowing incoming utility power to be "bypassed" to the UPS output during overload conditions or in the event of a UPS failure.

Convert polluted power to clean power

The double-conversion on-line UPS is ideal for solving power problems emanating from utility or generator power: Its design allows for the conversion of "polluted" power to clean power.

U.S. Air Force photo/Staff Sgt. Joshua J. Garcia

Figure 1 shows a typical “polluted” AC power waveform from a low-cost generator. Figure 2 shows the actual clean output waveform of an on-line UPS that was powered by the polluted generator power in Figure 1. Notice the:

1. Voltage dropouts
2. Noise and harmonics
3. Waveform distortion
4. Frequency instability [A and B durations between AC sinewaves (frequency) vary.]

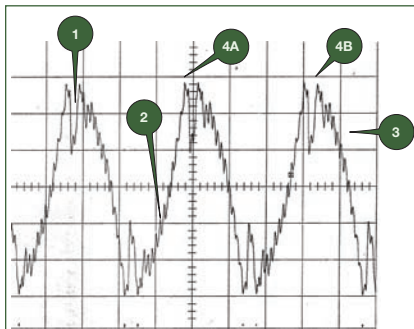


FIGURE 1: A typical “polluted” AC power waveform from a low-cost generator.

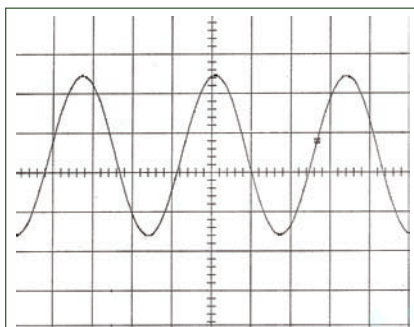


FIGURE 2: The clean output waveform of an on-line UPS that was powered by the polluted generator power in Figure 1.

No-break power capabilities

When the utility power is lost, the connected battery supply simply takes over as the energy source without the switch-over voltage dropouts associated with other low-cost off-line or line-interactive UPS designs.

The UPS output shown in Figure 1, 4A and 4B, defines a time duration of 1 Hz of AC power. For 60 Hz domestic power, the duration of 1 Hz is 16.66 milliseconds. A true double-conversion, on-line UPS has no break in output power should a loss of utility power occur as the battery simply takes over as the power source. Additionally, as the on-line UPS has a continuous-duty inverter circuit, extended or long-term battery mode operation is not a problem.

AC output voltage regulation

Because the on-line UPS is regenerating new AC power while operating from both utility and battery sources, a continuous ± 2 percent or better output voltage regulation is typically maintained. When the UPS is operating from a utility or generator source, the ± 2 percent output voltage regulation is maintained over the entire input voltage range of the UPS. This assures protection against sustained utility brown-outs and overvoltage conditions while maintaining the optimum voltage and power levels to the connected critical equipment.

Surge, transient, and overvoltage protection

The on-line UPS design places several layers of active electronic circuitry between the incoming utility power source and sensitive equipment. This results in a superior level of surge, transient, and overvoltage protection for equipment.

In contrast, off-line and line-interactive designs do not provide these active layers of electronics, depending instead on low-cost surge protection devices with limited capabilities. In overvoltage conditions, they switch to battery operation, limiting their operational time under this condition. In locations where the over- or under-voltage conditions repeatedly occur, the off-line and line-interactive UPS batteries can become totally discharged and render the UPS useless.

Frequency regulation

Most on-line UPS units ship configured with their output frequency set to be synchronized with the frequency of the incoming utility power. In most domestic applications this is acceptable. However, where the incoming power is provided by a generator, the UPS should be configured to have a fixed-frequency or nonsynchronized output. Generator sources are notorious for frequency drift and shifts, which, if passed through the UPS, can cause some equipment to operate unreliably. Configuring the on-line UPS for nonsynchronized operation provides protection against this problem. Meanwhile, since off-line and line-interactive UPSs pass incoming utility power directly through to the connected equipment, they are unable to provide any protection against incoming generator frequency problems.

Frequency conversion

Some on-line UPS models take the non-synchronized mode of operation further

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and are designed to operate as a true frequency converter, providing 50, 60, and 400 Hz output frequency irrespective of the input frequency. On-line UPS technology has been used as 400 Hz to 60 Hz frequency converters in some KC-135 Stratotankers. They change the 400 Hz generated by the aircraft's power to 60 Hz single-phase power for powering add-on computers and microwave-based electronic warfare subsystems. Off-line or line-interactive UPSs cannot be used for frequency conversion applications.

Input power factor correction

Most computer-based electronics today incorporate internal switch-mode power supplies. The input circuitry of these supplies typically consists of a basic rectifier and filter capacitor stage. One characteristic of these designs is a nonlinear current draw from the connected utility power. This is caused by the large input filter capacitors gulping charging current near the peaks of the AC waveform. In aircraft or buildings where multiple pieces of equipment are being powered from the same source or electrical panel, the current harmonics being generated by these nonlinear loads can rise to levels that cause excessive wiring heating or nuisance circuit breaker tripping. The harmonics can also be disruptive to networks, computers, and other sensitive electronics operating from the same power system.

A typical on-line UPS uses the same input rectifier and filter stage as a switch-mode power supply. However, many models are available with an additional input Power Factor Correction (PFC) circuit. The input PFC circuit senses the incoming voltage and current waveform and adjusts to maintain their phase relationships, eliminating most nonlinearities. Any equipment connected to the UPS output will also have its input power factor corrected.

Some military COTS requirements specify that equipment being supplied meets conducted emissions standard CE102. The standard states that the equipment will cause less than 3 percent current distortion (at any single harmonic) to be conducted back onto the incoming power source. Engineers should be aware that even though the COTS on-line UPS has input power factor correction, it probably will not meet the CE102 specifications due to the low-cost circuitry used.

Phase conversion

Some COTS on-line UPS models will accept a 400 Hz three-phase source while providing 60 Hz single-phase output. Small 400 Hz portable and aircraft-generation systems are sensitive to phase load imbalance. If an acceptable load balance is not maintained between the phases, power system harmonic levels can increase to a level that causes circuit breakers to "nuisance trip" and motors to overheat. Also, the harmonics can be disruptive to sensitive equipment operating from the same power bus. As more and more COTS single-phase equipment is installed as a low-cost solution, phase balancing is often not easily achievable. A COTS three-phase to single-phase UPS or phase converter is the ideal solution to these problems. These units allow the connection of one or more pieces of single-phase, 115-120 VAC, 50, 60, or 400 Hz equipment while drawing a balanced amount of power from a 400 Hz three-phase source.

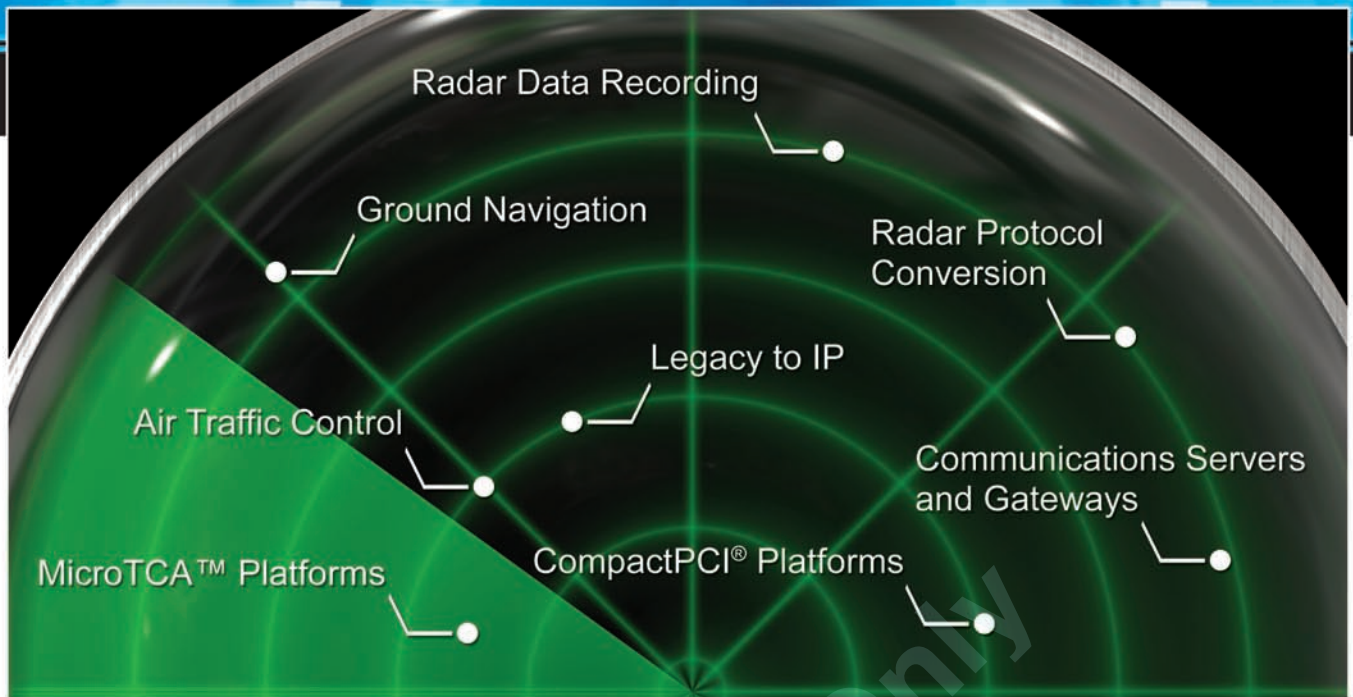
Double-conversion: An effective remedy

Double-conversion on-line technology is a flexible COTS platform. Either used directly off-the-shelf or modified by the UPS manufacturer, it can provide a fast, cost-effective solution to difficult power problems that may not be easily solved by other methods. ✚



Michael A. Stout is VP of Engineering at Falcon Electric, Inc. based in Irwindale, Calif. He is an authority on military and commercial computer power conversion and UPS systems, having more than two decades of experience. In his current position, Michael specifies and designs new UPS and critical power system products and evaluates emerging technologies. He can be reached at mstout@falconups.com.

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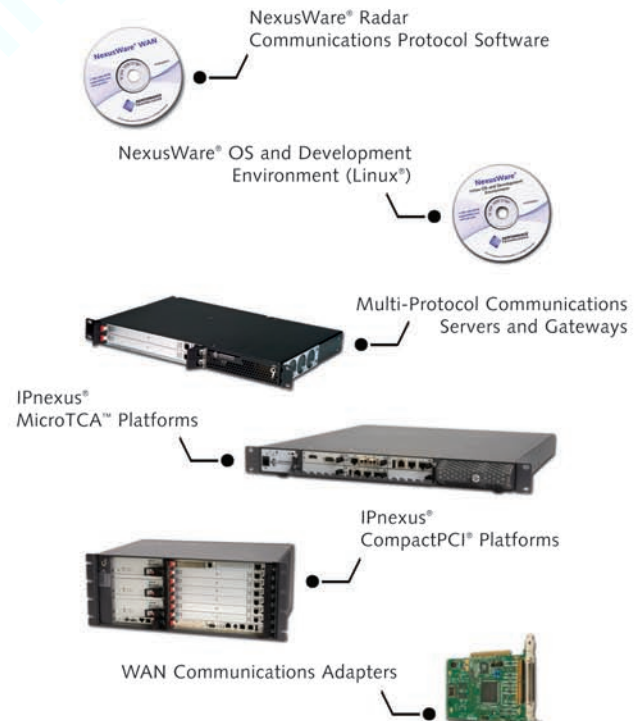


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Portable power management for soldiers: Fuel cell hybrid system is lighter, safer

By Dr. Peter Podesser

A fully integrated fuel cell/battery hybrid system offers the army a safe, lightweight power source for nonstop equipment operation by soldiers in the field as an alternative to carrying extra batteries and recharging systems.

The rising deployment of electronic equipment for soldiers in the field – from night-vision goggles, laptops, and communication devices to GPS and sensors – has increased the army's need for lightweight, reliable, and portable electrical power. But there are significant technical and logistical challenges to efficiently equipping soldiers with the power they need to run this equipment.

Because their devices must be operated autonomously, soldiers typically have to carry up to 30 lbs of various primary and backup batteries, depending on the power requirements of their individual devices. This adds considerably to the weight of the equipment and provisions they also must pack. But what if soldiers could carry a single lightweight power-conversion device that is able to adapt to the power needs of all their equipment? Such a power-conversion device should enable them to use any available power source in the field – generators, field chargers, solar panels, fuel cells, and so on – to recharge their batteries.

Now, a new fully integrated, lightweight fuel cell/battery hybrid system that offers this power-conversion flexibility and enough capacity to support a 72-hour mission has been developed for defense organizations in North America and Europe. Critical missions no longer have to be interrupted for battery replacements or recharges, and important systems do not fail anymore due to empty batteries. All these factors significantly increase the soldier's safety and effectiveness.

The Direct Methanol Fuel Cell (DMFC) system – which includes a fuel cell, fuel cell cartridge, and power manager – can reduce battery weight by up to 80 percent while providing improved logistics and increased safety for soldiers.

Portable hybrid power for soldiers

These hybrid, portable DMFC systems comprise three components that work together to provide a portable, flexible, reliable power source for today's armies: the fuel cell, the fuel cartridge, and the power manager.

Component 1 – The fuel cell

Fuel cells are increasingly being viewed as a reliable, versatile power source for defense applications. They offer a range of logistical, security, and functionality advantages in the field that soldiers appreciate: They operate almost silently without producing exhaust, they are immune to extreme weather, and they produce power only when needed. Unlike batteries, which just store energy, DMFCs are actual power generators, chemically converting a fuel into electrical power in one efficient step.

In the stack, the fuel cell's power-producing heart, a mixture of methanol and water is introduced to the anode side, which is connected to the cathode by an electrical circuit (Figure 1). A patented water management system enables use of 100 percent pure methanol in the fuel cartridges. (This also helps reduce the unit's weight because pure methanol has a very high energy density.) Ambient air is pumped into the stack on the cathode side. Upon contact with a platinum

catalyst, methanol releases its electrons, which flow in the direction of the cathode, thus producing power. At the same time, protons are released and penetrate the membrane to the cathode. There, the oxygen reacts with the proton and electrons to form pure water.

During this chemical process, the fuel cell releases water in the form of water vapor and carbon dioxide. The process is environmentally friendly: The amounts of water vapor and carbon dioxide produced are comparable to the breath of a child.

The most up-to-date of these portable DMFCs – used by army organizations in the U.S. and Europe – weighs only 3.7 lbs and measures 10" x 7" x 3". It provides

25 W continual nominal power directly to electrical devices or for charging secondary batteries. Its nominal voltage is 16.8 V, and it can be adapted to other voltages. (Output voltage is 10 to 30 VDC.) Fuel consumption at 25 W is less than 0.8 grams per watt-hour, which translates into an energy density of greater than 1,250 Wh/kg – roughly 10 times the energy density of Li-ion batteries. When connected to a rechargeable battery, the fuel cell will constantly monitor the battery's charge state. Once this drops below a predefined value, the fuel cell will automatically start recharging the battery. When the battery is full, the fuel cell returns to standby mode. This continuous power generation process enables longer dismounted missions for soldiers without

SFC systems win first and third prizes in DoD competition

Two portable fuel cell systems featuring SFC technology won first and third prizes in the first Wearable Power Prize Competition sponsored by the U.S. Department of Defense. The 2008 competition, which drew 170 entrants, was designed to encourage innovation in performance and weight reduction for energy systems carried by personnel during field missions.

The systems were evaluated in both bench tests and in simulated field-mission conditions. Attached to a standard military vest, they were required to provide 20 W of average electric power for 96 hours, meet brief peak-power demands up to 200 W, and weigh no more than 4 kg (8.8 lbs).

SFC entered two systems in collaboration with its U.S. partners. The prototype of the M-25 Portable Fuel Cell System, a joint project with DuPont, won the \$1 million first prize. SFC's commercially available portable Jenny fuel cell, entered with Capitol Connections LLC, won \$250,000 for third prize. The M-25 and the Jenny can power equipment such as GPS navigation devices, communications equipment, computers, sensors, C4ISR gear, robots, and UAVs – and weighs up to 80 percent less than conventional power sources.

the need to interrupt the mission for battery replacements or recharges, and significantly reduces the battery weight they must carry.

For example, a soldier who needs 25 W during a 72-hour mission would have a total power requirement of 1,600 watt-hours. Nine military batteries such as Type BA5590 (210 watt-hours per battery) are needed to provide that energy. Each battery weighs 2 lbs, so at a minimum a soldier would have to carry 18 lbs purely to satisfy these power needs. But soldiers often carry more than one type of battery, because their devices require different voltages.

So to be assured of the necessary energy for a 72-hour mission, a soldier would have to carry approximately 30 lbs of batteries. An example of an applicable technology is the Jenny fuel cell from SFC Smart Fuel Cell, which weighs only 3.7 lbs, plus a 1-lb power manager (Figure 2). This combination, plus the hybrid solution's five 0.8-lb fuel cartridges, would reduce the weight of the soldier's power supply by 65 percent compared to primary, or nonrechargeable, batteries. Secondary, or

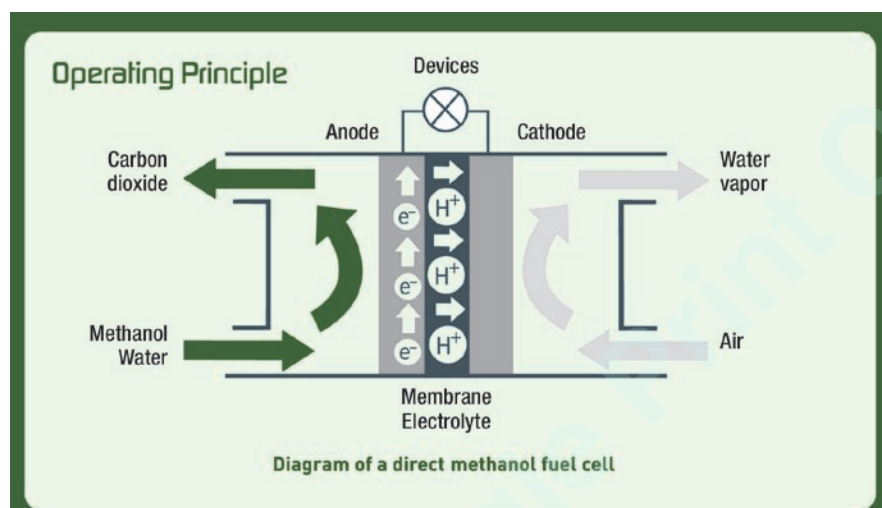


FIGURE 1: Unlike batteries, which just store energy, Direct Methanol Fuel Cells (DMFCs) are actual power generators, chemically converting fuel into electrical power in one efficient step.



FIGURE 2: The Jenny fuel cell from SFC weighs only 3.7 lbs, plus a 1-lb power manager.

rechargeable, batteries have even less energy density while weighing more. The hybrid fuel cell system is 80 percent lighter, on the average, than secondary batteries with equivalent power.

Component 2 – The fuel cartridge

DMFCs use methanol as a fuel, a liquid alcohol that is easy to store, transport, and ship – unlike the hydrogen gas used in hydrogen fuel cells. Methanol's most important property, however, is its extremely high energy density. Ten liters of methanol at a weight of approximately

18 lbs provides 11 kWh of power, a lot of energy at very low weight.

By comparison, a hydrogen tank of equivalent capacity is about five feet tall, weighs 187 lbs, and cannot be transported by aircraft. An equivalent-power battery system would weigh nearly 600 lbs.

Fuel for the Jenny fuel cell comes in convenient lightweight cartridges, each containing nearly 10 ounces of fuel at a weight of 0.6 lbs. Fuel cartridges can be easily exchanged during operation (hot swap).

“ Ten liters of methanol at a weight of approximately 18 lbs provides 11 kWh of power, a lot of energy at very low weight. By comparison, a hydrogen tank of equivalent capacity is about five feet tall, weighs 187 lbs, and cannot be transported by aircraft. ”

Component 3 – The power manager

Part of the hybrid DMFC system, the power manager, provides excellent operational flexibility to soldiers. Measuring 1.6" x 3.4" x 5" and weighing 1 lb, it enables efficient battery charging in the field by harvesting and efficiently managing energy from virtually any energy source to provide electrical power during operation of host equipment. Possible power sources include batteries of various chemistries and states of charge, fuel cells, photovoltaic cells, typical battery chargers, or automotive battery buses.

The power manager accepts a very wide range of input voltages (operational ranges: 30 VDC nominal: 22 to 24 VDC; 12 VDC: 10 to 32 VDC), and its output voltages (operational range: 10 to 24 VDC) are compatible with virtually any electrical equipment used by army organizations like night-vision goggles, laptops, communication, and GPS devices and sensors. The power manager will automatically adjust to the required output voltage by means of an implemented cable identification feature. This allows soldiers in the field to make optimum use of any available energy source for the duration of their mission.

Hybrid power system provides army advantages

As mentioned, the DMFC hybrid system provides distinct advantages to soldiers on the ground: reduced weight, improved logistics, and increased safety.


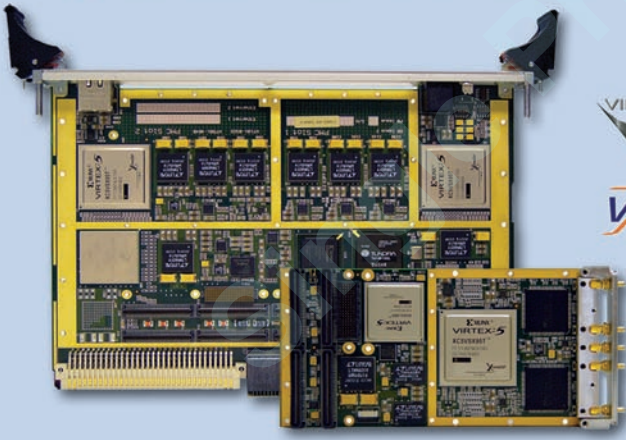
Significantly reduced weight

With the use of the fuel cell/fuel cartridge/power manager hybrid system, the weight to be transported can be reduced by 65 percent compared to primary, non-rechargeable batteries and up to 80 percent compared to secondary, rechargeable batteries as discussed previously.

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Improved logistics

Battery logistics can present a formidable challenge, as seen in the war in Iraq. Army organizations still prefer primary batteries to secondary batteries for a number of reasons: They offer long shelf life, they are easy to use, and they are immediately available without charging and priming. Their downside, however, is that once they are empty, they need to be discharged and replaced – both of which can be a challenge in critical situations. Secondary batteries can be recharged and thus reused many times, which poses less of a logistical challenge. However, severe problems arise if there are no available charge stations. With the portable power hybrid solution, however, all that soldiers need is always in their vests; with the fuel cell they have a personal power generator, and with the rechargeable battery they have power storage. Fuel for several days (25 W continuous for 72 hours: five 0.8 lb cartridges) can be easily packed and transported, making the soldier independent of logistics support.

Increased soldier safety

Direct methanol fuel cells contain no hazardous components. Defense organizations in the U.S. and Europe have rigorously tested methanol fuel to determine whether it would catch fire or explode. During these tests, rounds of different types of ammunition were fired at SFC fuel cartridges and at materials soaked in methanol. The methanol did not catch fire in any tests.

Hybrid power system keeps pace with technology

Technology has provided the army with advanced equipment for more efficient and safer field missions, but until recently the available power sources had not kept pace with those advances. DMFCs combined in a fully integrated fuel cell/battery hybrid system have enabled soldiers to take advantage of this advanced equipment while reducing the weight they are required to carry. In situations when it really counts, soldiers having their own power system with them can make a major difference. Critical missions no longer have to be interrupted for battery replacements or recharges, and important systems do not fail anymore due to empty batteries. All these factors significantly increase the soldier's safety and operability. +



Dr. Peter Podesser was named CEO of SFC Smart Fuel Cell in November 2006. He has more than 20 years of management and executive experience with technology companies in Europe, the U.S., and Asia. Previous work experience includes management positions in sales and marketing for RHI AG. Peter has also served as president and CEO of EV Group and as president of Unaxis's Wafer Processing Division. He studied business administration and languages at the University of Economics and Social Sciences in Vienna, and earned a Ph.D. in Strategic Planning from the university. He can be contacted at pr@sfc.com.

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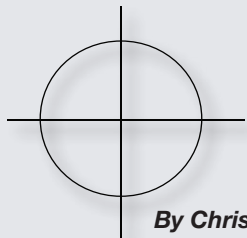


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By Chris A. Ciufo, Editor

DO-254: The other safety-critical specification



Editor's Note: Next month's edition of *Military Embedded Systems* has our annual "FPGAs and Reconfigurable Computing" supplement, which is part of sister publication DSP-FPGA.com. To whet your appetite, I thought it very appropriate to focus on a thin slice of the FPGA design problem that sometimes vexes military system designers: safety-critical hardware certification.

By now you're probably aware that the FAA's RTCA/DO-178B "Software Considerations in Airborne Systems and Equipment Certification" governs software certified for airborne systems ranked from levels E through A (the highest). DO-178B's rigorous test methodology makes darn certain that the software controlling the flight surfaces in an avionics system exhibits *no possible aberrant behaviors* and doesn't use poor coding practices such as undefined variables or priority inversions.

But did you know there's a companion spec for hardware called RTCA/DO-254 "Design Assurance Guidance for Airborne Electronic Hardware"? This spec got much more attention five years ago when it was updated to Advisory Circular AC.20 DO-254 to specifically include the FPGAs that are integral to the Joint Tactical Radio System (JTRS). Since then, vendors Aldec and Mentor Graphics want designers to know how to create safety-critical FPGA-based defense systems.

Mentor Graphics, a broad line EDA tools company that even has its own RTOS (Nucleus), is the 800-pound gorilla in this market. Most defense designers feel more comfortable talking about VPX conduction-cooled boards or Ethernet LANs than they do about IC designs and EDA tools. And Mentor is well aware that the Aerospace and Defense (A&D) markets don't need many of the products in the company's arsenal. But when it comes to safety-critical systems – especially those using FPGAs – Mentor offers some worthwhile advice to achieve DO-254 design assurance levels from E to A.

The biggest issue, says Michelle Lange, Mentor's DO-254 program manager, is risk. At the FPGA Summit held in late Fall 2008, I moderated a panel session where Lange was one of the key participants. DO-254, she said, adds "significant time, risk, and cost to design projects." The 25 to 400 percent cost increase – and the risk of failing a certification audit and having to redesign (and rewrite code) – are the biggest reasons for tools from companies like Mentor or Aldec. DO-254's requirements-based approach is similar to DO-178B for software. The FPGA design must capture and validate requirements, design to those requirements, and then verify that the design meets them. Sounds simple, right?

By their nature, FPGAs are a blank canvas into which RTL is applied, a design synthesized, and logic realized. There are infinite variations and countless iterations to get a design working in the

first place, not to mention it fitting within available logic and then pinning out to the circuit board ... thus the following four tips:

Hot Tip #1: To achieve a DO-254 certified design, the trick is proper preparation and a structured design process. Mentor advises that seeking out DO-254 certification training is well worth the cost involved, even for a large design team. This avoids missteps and rework, especially on the fixed-price programs more common in a global recession and in DoD Secretary Gates' "new approach" to contracting.

Hot Tip #2: Plan for requirements management and traceability as part of the process. As *Military Embedded Systems* readers have seen on the software side with tools from IBM/Telelogic and others, software is available to help capture design requirements – even across a geographically distant design or sub-contracting team. The heart of DO-254 is stating, designing to, and verifying compliance with requirements. Use a tool that automates the requirements creation process. Don't forget about configuration management and artifacts generation during the design stage: You'll need them later. Altera, for instance, has a DO-254 ecosystem for its products and even offers the NIOS II_SC as soft IP that's "certifiable to DO-254."

Hot Tip #3: When it comes to chapter 6.2 of DO-254 – verifying the design – there are myriad choices from Altera, Xilinx, Mentor, and GateRocket. Aldec, for instance, promises at-speed hardware verification and "golden" vectors. The company uses a combination of software and hardware boards to exercise speed-accurate designs.

But whichever tool or flow is used, make sure the verification process maps back to the requirements necessary to achieve DO-254 certification. Verifying a functional design is one thing, but in this case, the design must be shown to also live up to the predefined requirements. Don't forget about configuration management and artifacts generation.

And finally, Hot Tip #4: Choose tools designed for safety-critical systems. I suppose you'd expect Mentor to say that since they're trying to sell tools. But while self-serving, it's really a round peg/round hole scenario. Verification companies like Aldec and Mentor have DO-254 certification success in mind with many of their products. Why choose tools that don't mesh with hardware certification?

More information can be found at:

Aldec: www.aldec.com/Technologies/Technology.aspx?technologyid=f61dbc4a-8072-49d1-bf7c-ac5590221acd

Altera: www.altera.com/end-markets/military-aerospace/do-254/mil-do-254.html

Mentor Graphics: www.mentor.com/go/do-254

Xilinx: www.xilinx.com/esp/aero_def/do254.htm

CV90 Armored Vehicle DDG-1000 Multi-Mission Destroyer Roland Air Defense System
HIMARS Artillery Rocket System B-2 Stealth Bomber F-35 Lightning II
LHD Class Amphibious Assault Ship Expeditionary Fighting Vehicle Gripen Fighter
Littoral Combat Ship A400M Transport NSSN Virginia Class Submarine
F-117 Stealth Fighter MEADS Air Defense System EMB-145 Challenger 2 Tank
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